PATENT **Docket No. Fuehrer 3-48-26-2**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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TITLE:	INDUCTIVE COUPLING FOR SILICON DATA ACCESS ARRANGEMENT	

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MAIL STOP APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Board of Patent Appeals and Interferences

APPELLANTS' BRIEF

This Appeal Brief is in furtherance of the Notice of Appeal filed in this case on April 17, 2007. The Commissioner is authorized to charge the fee for filing of this Appeal Brief to Deposit Account No. 19-5425.

1. REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc, a subsidiary of LSI Corporation. Accordingly, LSI Corporation is the real party in interest.

2. RELATED APPEALS AND INTERFERENCES

The Appellants, assignee, and the legal representatives of both are unaware of any other appeal or interference which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

3. STATUS OF CLAIMS

A. Claims canceled: 7, 8, 17, 24, 31, and 32

B. Claims withdrawn from consideration but not canceled: None

C. Claims pending: 1-6, 9-16, 18-23, 25-30 and 33-38

D. Claims allowed: none

E. Claims rejected: 1-6, 9-16, 18-23, 25-30 and 33-38

F. Claims appealed: 1-6, 9-16, 18-23, 25-30 and 33-38

Appealed claims 1-6, 9-16, 18-23, 25-30 and 33-38 as currently pending are attached as the Claims Appendix hereto.

4. STATUS OF AMENDMENTS

A Reply under 37 C.F.R. §1.112 was filed on May 31, 2005; claim amendments were made. In response, the Examiner entered the claim amendments and issued a non-final Office Action on August 15, 2005. A Reply under 37 C.F.R. §1.112 was filed on December 15, 2005: no claim amendments were made. In response, the Examiner issued a non-final Office Action on March 14, 2006. A Reply under 37 C.F.R. §1.112 was filed on July 14, 2006: no claim amendments were made. In response, the issued final Office Action on September 26, 2006. A Reply under 37 C.F.R. §1.116 was filed on December 22, 2006: no claim amendments were made. In response, the Examiner issued the final Office Action appealed herein on April 17, 2007.

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claim 1: An electrical interface, comprising: a codec that generates two signal paths that together form an input differential pair (page 5, lines 25-26); a primary inductor and a secondary inductor for operably coupling said input differential signal pair to an output differential signal pair (page 5, lines 26-27), a filter that attenuates a signal occurring in the output differential signal pair (page 6, lines 23-26); and a parasitic capacitor operably coupled between the primary inductor and the secondary inductor, wherein the parasitic capacitor has a capacitance in the range of approximately 0.5 pF to approximately 2.5 pF (page 6, lines 14-17 and 21-22).

Claim 21: An electrical interface, comprising: a differential driver means for generating two signal paths that together form an input differential signal pair (page 5, lines 25-26); inductive means for operably coupling said input differential signal pair to an output differential signal pair (page 5, lines 26-27), the inductive means including a parasitic capacitor, said parasitic capacitator having a capacitance in the range of approximately 0.5 pF to approximately 2.5 pF (page 6, lines 14-17 and 21-22); and filter means for attenuating a signal occurring in the output differential signal pair (page 6 lines 23-26).

Claim 30: A method of interfacing an input differential signal pair to an output differential signal pair, the method comprising: inductively coupling the input differential signal pair to an output differential signal pair (page 5, lines 25-27), and filtering out a common mode signal occurring in the output differential signal pair (page 6 lines 23-26); wherein the inductively coupling step further includes the step of capacitively coupling at least one input signal in the input differential pair to at least one output signal in the output differential signal pair (page 5, lines 26-27); and wherein the step of capacitively coupling is performed with a capacitance in the range of approximately 0.5 pF to approximately 2.5 pF (page 6, lines 14-17 and 21-22).

The present invention improves the attenuation of an undesired signal found in a differential signal path by using inductive, as opposed to capacitive, coupling. The inventive electrical interface includes a primary inductor, a secondary inductor, and a filter. The

primary inductor and the secondary inductor operably couple an input differential signal pair to an output differential signal pair, and the filter attenuates an undesired signal in the output differential signal pair. The input differential pair is formed by using a differential driver, e.g., a CODEC, to generate the pair from a single input line (e.g., a tip line).

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellants request the Board to review the following rejections:

1. Rejection of Claims 1-6, 9-19, 21-23, 25-30 and 33-37 under 35 U.S.C. §103(a) based on U.S. Patent No. 6,212,263 to Sun et al. in view of U.S. Patent No. 6,137,392 to Herbert et al. and further in view of U.S. Patent No. 4,401,955 to Yorinks et al.

7. ARGUMENT

The Cited Art Does Not Render the Claims Obvious

The Examiner Has Not Established a P*rima Facie* Case of Obviousness

As set forth in the MPEP:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143

The present invention claims the use of a parasitic capacitor between the primary inductor and the secondary inductor, and using a capacitance value for the parasitic capacitor

that is as small as possible while still preventing common mode noise signals from interfering with signals being transmitted over the input differential pair. In a preferred embodiment, this capacitance value is in a range of approximately 0.5 pF to approximately 2.5 pF. This claimed combination improves the attenuation of an undesired signal found in a differential signal path by using inductive, as opposed to capacitive, coupling.

As the Examiner has acknowledged that Sun fails to teach a capacitance operably coupled between the primary inductor and the secondary inductor, the focus of this argument turns to the Examiner's assertion that Herbert teaches a capacitor coupled between the primary and secondary inductors for the purpose of obtaining a high dielectric isolation, and the Examiner's assertion that Yorinks teaches a filter capacitor in the range of approximately 0.5 to approximately 2.5 pF.

The Examiner looks to Herbert to teach a capacitance operably coupled between the primary inductor and the secondary inductor and provide motivation for including this as an added feature to the system provided by Sun. The Examiner says it would be obvious to modify the transformer taught by Sun (shown in Sun, Fig. 6) to include a parasitic capacitor operably coupled between the primary inductor and the secondary inductor as taught by Herbert "to provide a high degree of noise isolation and safety" (page 7 of Office Action). However, these results arise from <u>the isolation and grounding of the interstage connection</u>, not the inclusion of a parasitic capacitor oeprably coupled between the primary inductor and the secondary inductor. Herbert provides no direct motivation for including a parasitic capacitor. Additionally, Sun does not include a capacitor coupled between the primary inductor and the

secondary inductor while still providing several grounding points to provide noise isolation and safety in the circuit. It is unclear why one would be motivated to add an additional component to Sun which results in features already provided for by Sun. At best, impermissible hindsight is being used to attempt to find a basis for rejecting the claimed invention under 35 U.S.C. §103. However, since fundamental teachings and/or suggestions, which would be required to make the rejections valid, are missing, the rejection of the claims must fail.

Secondly, the Examiner looks to Yorinks to teach the capacitor has a capacitance in the range of approximately 0.5 pF to approximately 2.5 pF. Yorinks is directed towards a power divider circuit used for receiving power transmitted over a coaxial line which utilizes a .5 pF capacitor in the disclosed circuitry. However, Yorinks provides no motivation for using a .5 pF capacitor in either the power supply circuit of Sun or the switched mode transformer of Herbert. Additionally, the Examiner provides no motivation from Yorinks to modify either Sun or Herbert. Again, the same motivation for combination is cited as before, "to provide a high degree of noise isolation and safety" (Action, page 7). Herbert teaches away from the present invention by including a system operating on a power scale that exceeds the power scale of the present invention by a factor of greater than 1000. Nowhere does Herbert suggest utilizing low capacitance components, such as the presently claimed parasitic capacitor. In fact, utilizing such a low capacitance in the combined system of Sun and Herbert would result in an extremely unsafe situation as the low rated capacitor would be unable to handle the high power levels. At best, impermissible hindsight is being used to attempt to find a basis for

rejecting the claimed invention under 35 U.S.C. §103. However, since fundamental teachings and/or suggestions, which would be required to make the rejections valid, are missing, the rejection of the claims must fail.

Since each of the independent claims specifically recite the minimization of the capacitance of the parasitic capacitor (Claims 1, 21, and 30 specifying the range of 0.5 pF to 2.5 pF and claim 38 specifying that the capacitance be minimized according to certain parameters), the claimed invention patentably defines over Sun, Herbert and Yorinks, whether considered alone or in any combination. Accordingly, this Board is respectfully requested to reconsider and withdraw the rejections of Claims 1-6, 9-19, 21-23, 25-30, and 33-38 under 35 U.S.C. §103.

8. CONCLUSION

For the foregoing reasons applicants respectfully request this Board to overrule the Examiner's rejections and allow Claims 1-6, 9-16, 18-23, 25-30 and 33-38.

Respectfully submitted,

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Date

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CLAIMS APPENDIX

CLAIMS INVOLVED IN THIS APPEAL:

1. (Previously presented) An electrical interface, comprising:

a codec that generates two signal paths that together form an input differential pair;

a primary inductor and a secondary inductor for operably coupling said input differential signal pair to an output differential signal pair,

a filter that attenuates a signal occurring in the output differential signal pair; and

a parasitic capacitor operably coupled between the primary inductor and the secondary inductor, wherein the parasitic capacitor has a capacitance in the range of approximately 0.5 pF to approximately 2.5 pF.

2. (Original) The interface according to claim 1, wherein the filter acts as a low-pass filter and wherein the electrical interface further includes a high-pass filter, the low-pass filter and the high-pass filter having overlapping cut-off frequencies.

3. (Original) The interface according to claim 2, wherein the low-pass filter and the high-pass filter together attenuate signals over a frequency range of approximately 50 kHz to approximately 10 MHz.

4. (Original) The interface according to claim 1, wherein the primary inductor is connected between two signal paths forming the input differential signal pair.

5. (Original) The interface according to claim 4, wherein the primary inductor forms the primary winding of a transformer.

6. (Original) The interface according to claim 5, wherein the secondary inductor is connected between two signal paths forming the output differential signal pair and wherein the secondary inductor forms the secondary winding of the transformer.

7. (Canceled)

8. (Canceled)

9. (Original) The interface according to claim 1, wherein the filter includes an output attenuation element for operably coupling a signal path of the output differential signal pair to ground.

10. (Original) The interface according to claim 9, wherein the output attenuation element includes a resistor and a capacitor connected in parallel.

11. (Original) The interface according to claim 9, wherein the output attenuation element forms a low-pass filter.

12. (Original) The interface according to claim 1, further including an input attenuation element operably coupled to at least one of the signal paths forming the input differential signal pair.

13. (Original) The interface according to claim 12, wherein the input attenuation element includes a resistor and a capacitor connected in series.

14. (Original) The interface according to claim 12, wherein the input attenuation element forms a high-pass filter.

15. (Original) The interface according to claim 1, wherein the filter attenuates a common mode signal in the output differential signal pair.

16. (Original) The interface according to claim 1, wherein the interface is adapted for being operably coupled between a codec and a digital circuit.

17. (Canceled)

18. (Previously presented) The interface according to claim 1, further including an analog front end for operably coupling the codec to a telephone line.

19. (Original) The interface according to claim 18, wherein the analog front end includes circuitry for providing power to the codec from the telephone line.

20. (Original) The interface according to claim 18, wherein the analog front end includes a shunt regulator.

21. (Previously presented) An electrical interface, comprising:

a differential driver means for generating two signal paths that together form an input differential signal pair;

inductive means for operably coupling said input differential signal pair to an output differential signal pair, the inductive means including a parasitic capacitor, said parasitic capacitor having a capacitance in the range of approximately 0.5 pF to approximately 2.5 pF; and

filter means for attenuating a signal occurring in the output differential signal pair.

22. (Original) The interface according to claim 21, wherein the filter means attenuates high-frequency signals and wherein the electrical interface further includes a high-pass filtering means for attenuating low-frequency signals, the filter means and the high-pass filtering means having overlapping cut-off frequencies.

23. (Original) The electrical interface according to claim 21, wherein the inductive means is a transformer.

24. (Canceled)

25. (Original) The interface according to claim 21, wherein the filter means includes an output attenuation element for operably coupling a signal path of the output differential signal pair to ground.

26. (Original) The interface according to claim 25, wherein the output attenuation element includes a resistor and a capacitor connected in parallel.

27. (Original) The interface according to claim 25, wherein the output attenuation element forms a low-pass filter.

28. (Original) The interface according to claim 21, further including an input attenuation means for attenuating low-frequency signals, the input attenuation means being operably coupled to at least one of the signal paths forming the input differential signal pair.

29. (Original) The interface according to claim 12, wherein the input attenuation element includes a resistor and a capacitor connected in series.

30. (Previously presented) A method of interfacing an input differential signal pair to an output differential signal pair, the method comprising:

inductively coupling the input differential signal pair to an output differential signal pair, and

filtering out a common mode signal occurring in the output differential signal pair; wherein the inductively coupling step further includes the step of capacitively coupling at least one input signal in the input differential pair to at least one output signal in the output differential signal pair; and

wherein the step of capacitively coupling is performed with a capacitance in the range of approximately 0.5 pF to approximately 2.5 pF.

31. (Canceled)

32. (Canceled)

33. (Original) The method according to claim 30, wherein the filtering step further includes the step of attenuating high frequency signals with a low-pass filter and attenuating low frequency signals with a high-pass filter, the low-pass filter and the high-pass filter having overlapping cut-off frequencies.

34. (Original) The method according to claim 33, further including the step of attenuating signals over a frequency range of approximately 50 kHz to approximately 10 MHz.

35. (Original) The method according to claim 30, wherein the inductively coupling step includes the step of coupling the input and output differential signal pair through a transformer.

36. (Original) The method according to claim 30, wherein the filtering step includes the step of attenuating high-frequency signals in the output differential signal pair.

37. (Original) The method according to claim 30, further including the step of attenuating low-frequency signals in the input differential signal pair.

38. (Previously Presented) An electrical interface, comprising:

a codec that generates two signal paths that together form an input differential pair;

a primary inductor and a secondary inductor for operably coupling said input differential signal pair to an output differential signal pair,

a filter that attenuates a signal occurring in the output differential signal pair; and

a parasitic capacitor operably coupled between the primary inductor and the secondary inductor, wherein the parasitic capacitor has a capacitance that is as small as possible while still preventing common mode noise signals from interfering with signals being transmitted over said input differential pair.

EVIDENCE APPENDIX

No additional evidence is presented.

RELATED PROCEEDINGS APPENDIX

No related proceedings are presented.